Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

Claims 1-14 (canceled)

15. (currently amended) A method for fabricating a circuit component, comprising:

providing a semiconductor wafer, a metal pad over said semiconductor wafer, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer on said second region and over said semiconductor wafer, wherein an opening in said passivation layer is over said ~~metal pad and~~ first region, and said first region is at a bottom of said opening; ~~exposes said metal pad, and a gold layer over said semiconductor wafer, wherein said gold layer is connected to said metal pad through said opening; and~~

providing an exposed metallization structure over said semiconductor wafer, over said passivation layer and on said first region, wherein said exposed metallization structure is connected to said first region through said opening, and wherein said exposed metallization structure comprises a metal bump used for a package interconnect; and

after said providing said exposed metallization structure, performing a sputter etching process with an argon gas. ~~ion milling said gold layer.~~

Claim 16 (canceled)

17. (currently amended) The method of claim 15, wherein said metal bump has a substantially vertical sidewall extending from a bottom of said metal bump to a substantially planar top surface of said metal bump. ~~ion milling said gold layer comprises using argon.~~

Claims 18-26 (canceled)

27. (currently amended) A method for fabricating a circuit component, comprising:

providing a semiconductor wafer, a metal pad over said semiconductor wafer, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer over said semiconductor wafer and on said second region, wherein an opening in said passivation layer is over said ~~metal pad and~~ first region, and said first region is at a bottom of said opening; ~~exposes said metal pad, and a noble metal layer over said semiconductor wafer,wherein said noble metal layer is connected to said metal pad through said opening; and~~

providing an exposed metallization structure over said semiconductor wafer, over said passivation layer and on said first region, wherein said exposed metallization structure is connected to said first region through said opening, and wherein said exposed metallization structure comprises a metal bump used for a package interconnect; and

after said providing said exposed metallization structure, performing an ion milling process ~~said noble metal layer~~ with an argon gas.

Claims 28 and 29 (canceled)

30. (currently amended) The method of claim 27, wherein said metal bump has a substantially vertical sidewall extending from a bottom of said metal bump to a substantially planar top surface of said metal bump. ~~ion milling said noble metal layer comprises using argon.~~

Claims 31-34 (canceled)

35. (currently amended) The method of claim 15, after said ~~ion milling said gold layer~~ performing said sputter etching process, further comprising contacting said ~~gold layer~~ metal bump with a testing probe.

36. (currently amended) The method of claim 27, after said ~~ion milling said noble metal layer~~ performing said ion milling process, further comprising contacting said ~~noble metal layer~~ metal bump with a testing probe.

37. (new) A method for fabricating a circuit component, comprising:

providing a semiconductor wafer, a metal pad over said semiconductor wafer, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer on said second region and over said semiconductor wafer, wherein an opening in said passivation layer is over said first region, and said first region is at a bottom of said opening;

providing an exposed metallization structure directly on said passivation layer, on said first region and over said semiconductor wafer, wherein said exposed metallization structure is connected to said first region through said opening, and wherein said exposed metallization structure comprises a metal bump used for a package interconnect; and

after said providing said exposed metallization structure, performing an ion milling process with an inert gas.

38. (new) The method of claim 37, wherein said inert gas comprises an argon gas.

39. (new) The method of claim 37, wherein said inert gas comprises an helium gas.

40. (new) The method of claim 37, wherein said metal bump has a substantially vertical sidewall extending from a bottom of said metal bump to a substantially planar top surface of said metal bump.

41. (new) The method of claim 37, after said performing said ion milling process, further comprising contacting said metal bump with a testing probe.